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Description

METHOD AND RELATED APPARATUS FOR DERIVING A TRACKING ERROR SIGNAL

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to a method for deriving a tracking error signal in an optical storage system, and more particularly, to a method for deriving a tracking error signal based on a first analog detection signal and a second analog detection signal.

[0003] 2. Description of the Prior Art

[0004] An optical pick-up head, which is used to access data, plays an important role in various optical storage systems. Taking an optical drive as an example, the basic infrastructure of the optical drive can be seen in Fig.1, which is a schematic diagram of a typical optical drive 10. The typical optical drive 10 includes a pick-up head 12, a spinning motor 14, and a movement stage 16. The pick-up

head 12 is used to focus an optical beam 18 on a surface of a recording carrier 20(an optical disk) to form an optical spot whose area is close to the data area of the optical disk 20. The spinning motor 14 rotates the optical disk 20.

[0005] Ideally, the optical spot propagates along a track direction on the optical disk 20 to form an optical spot trace 22 to access data on the optical disk 20. The pick-up head 12 is connected to the movement stage 16, and the movement stage 16 can assist the pick-up head 12 to seek tracks, so that the pick-up head 12 can move appropriately to a target track on the optical disk 20 to read or to write data. Taking a data-reading process as a brief example, after the optical beam emitted from the pick-up head 12 is reflected and refracted from an information plane of the optical disk 20, an optical sensor will receive the reflected (refracted) light. According to the different areas on the optical disk 20 respectively representing 0 and 1, the reflected light will show different optical intensities. The optical sensor will transform the reflected light of the different optical intensities into corresponding voltage signals.

[0006] When the optical drive 10 operates, the optical disk 20 is rotated at a very high frequency. Operating characteristics

of the optical disk 20 in such circumstances are prone to be highly temperature-dependent and external-force-dependent. In addition, due to the optical disk 20 being a detachably installed recording carrier, the rotating center of the optical disk 20 may deviate from the predetermined center of rotation, so that the optical disk 20 may operate unstably, causing focus errors and tracking errors. Therefore, the pick-up head 12 is required to lock the optical spot along the desired data track on the optical disk 20 to accurately and quickly access data.

[0007] Moreover, the optical disk 20 shown in Fig.1 is used to store high-density data, so that the width of the data tracks and distance between the data tracks are both very short. Therefore, any deviation from the data track will lead to incorrect data accessing. When being practically implemented, the optical spot emitted from the optical pick-up head should be perfectly located at the data track.

[0008] Please refer to Fig.2, which is a schematic diagram showing a spatial relationship between a data track on the optical disk 20 shown in Fig.1 and an optical sensor 30 of the pick-up head 12. A plurality of pits 32 of different lengths are strewn along the data track. An arrow mark 34

shown in Fig.2 represents a track direction of the data track on the optical disk 20, and the optical sensor 30 of the pick-up head 12 moves and accesses data along the arrow mark 34 on the optical disk 20. The optical sensor 30 is a four-dimensional sensor, including a section A, a section B, a section C, and a section D. When each pit 32 on the data track passes through the optical sensor 30 of the pick-up head 12, the optical sensor 30 can be used to receive the optical beam 18 reflected and refracted from the pit 32. A tracking error signal TE and a focus error signal FE are generated according to four received different portions in space of the optical beam 18 respectively corresponding to the four sections (the section A, the section B, the section C, and the section D) of the optical sensor 30. The tracking error signal TE represents a deviation of the optical spot away from the data track. The focus error signal FE represents a distance between a focal point of the optical beam 18 shown in Fig.1 and the information plane of the optical disk 20. According to the tracking error signal TE and the focus error signal FE, the position of the optical pick-up head 12 can be dynamically adjusted. Some prior art patents whose subject is aimed at generating the tracking error signal TE based on

the above-mentioned optical sensor 30 are discussed below.

[0009] In US Patent No. 4,057,833, "Centering detection system for an apparatus for playing optically readable recording carriers", Braat et al. utilize an all analog technique to generate a plurality of corresponding output signals according to the plurality of portions of the optical beam. Braat et al. then make use of time differences or phase differences among those output signals to generate the tracking error signal TE.

[0010] For increasing the accuracy of generated signals, Bakx et al. teach an all digital approach to process data in US Patent No. 6,137,755, "Deriving a tracking error signal from a time difference between detector signals". Regarding the structure disclosed by Bakx et al, please refer to Fig.3, which is a functional block diagram of a tracking error signal generator 40 according to the prior art. As shown in Fig.3,the tracking error signal generator 40 includes two signal input ports (a first signal input port 42 and a second signal input port 44), two digitizers (a first digitizer 46 and a second digitizer 48), a digital delay device 50, two comparators (a first comparator 52 and a second comparator 54), and a signal generator 56. The

first signal input port 42 is used to receive a first analog detection signal A1 and the second signal input port 44 is used to receive a second analog detection signal A2.

[0011] Please also refer to Fig.2. The four detecting sections A, B, C, D of the optical sensor 30 can be used to respectively generate four corresponding output signals a, b, c, d, according to corresponding portions of the optical beam. If there is a deviation between the optical spot and the data track, there are time differences between the output signals a, b, c, d. For clarifying the degree of the deviation, a first analog detection signal A1 is set as a sum of the output signal a and the output signal c (A1=a+c), and a second analog detection signal A2 is set as a sum of the output signal b and the output signal d (A2=b+d). Please continue to refer to Fig.3. The first signal input port 42 and the second signal input port 44, which are respectively connected to first digitizer 46 and second digitizer 48, are respectively used to transform the first analog detection signal A1 and the second analog detection signal A2 into a first digital detection signal D1 and a second digital detection signal D2.

[0012] Please refer to Fig.4 that is a time sequence diagram showing variations of a plurality of signals generated in

Fig.3. As shown in Fig.4, there is a time difference Δ between the first digital detection signal D1 and the second digital detection signal D2, and the time difference Δ represents the deviation between the optical spot and the data track.

[0013] Please return to Fig.3. The digital delay device 50 is electrically connected to the first digitizer 46 for digitally delaying the first digital detection signal D1 with a delay time Td to generate a digital delay signal DR. Afterwards, the digital delay signal DR and the first digital detection signal D1 will pass through the first comparator 52 to generate a first digital comparing signal DC1. The first comparator 52 can be an XOR (Exclusive OR) logic gate and mainly used to extract front edges and rear edges of the digital delay signal DR and the first digital detection signal D1. Similarly, the digital delay signal DR and the second digital detection signal D2 pass through the second comparator 54 (an XOR logic gate) to generate a second digital comparing signal DC2, and the first digital comparing signal DC1 and the second digital comparing signal DC2 are both shown in Fig.4. The first comparator 52 and the second comparator 54 are jointly connected to the signal generator 56. The signal generator 56 can be

used to subtract the first digital comparing signal DC1 from the second digital comparing signal DC2 to generate a time-difference signal DT.

[0014] According to the time-difference signal DT, the related circuitry can discriminate the relationship between the first digital detection signal D1 and the second digital detection signal D2 in time domain. As shown in Fig.4, the time-difference signal DT is a negative voltage value that represents that the first digital detection signal D1 transcends the second digital detection signal D2. Afterwards, the signal generator 56 can be used to process the time-difference signal DT to generate the tracking error signal TE. Therefore, the optical spot emitted from the optical pick-up head 12 shown in Fig.1 can dynamically move along the track direction shown by the arrow mark 34in Fig.2 according to the tracking error signal TE.

[0015] Another structure disclosed in prior art patents is shown in Fig.5, which is a functional block diagram of a tracking error signal generator 60. The difference between the embodiment of Fig.5 and that of Fig.3 is that the Fig.5 embodiment includes four signal input ports 62. Without executing a signal combination process, the four signal input ports 62 directly and respectively receive the four cor-

responding output signals a, b, c, d generated by the four detecting sections A, B, C, D of the optical sensor 30 shown in Fig.2. The four corresponding output signals a, b, c, d can be respectively treated as a first analog detection signal A1, a second analog detection signal A2, a third analog detection signal A3, and a fourth analog detection signal A4 in the tracking error signal generator 60. Except for the above-mentioned difference, all the other characteristics of this embodiment, including the all digital operations, are the same as in the previous one.

[0016] The tracking error signal generator 60 further includes four digitizers 64, which are respectively electrically connected to the four signal input ports 62 and are used for respectively transforming the first analog detection signal A1, the second analog detection signal A2, the third analog detection signal A3, and the fourth analog detection signal A4 into a first digital detection signal D1, a second digital detection signal D2, a third digital detection signal D3, and a fourth digital detection signal D4. The embodiment shown in Fig.5 includes two first digitizers 70 used for respectively delaying the first digital detection signal D1 and third digital detection signal D3 into a first digital delay signal DR1 and a third digital delay signal DR3. Sim-

ilar to Fig.3, four comparators 68 (XOR logic gate) can be used. The first digital delay signal DR1 can be compared with the first digital detection signal D1 to generate a first digital comparing signal DC1. The first digital delay signal DR1 can also be compared with the second digital detection signal D2 to generate a second digital comparing signal DC2. The third digital delay signal DR3 can be compared with the third digital detection signal D3 to generate a third digital comparing signal DC3. In addition, the third digital delay signal DR3 can be compared with the fourth digital detection signal D4 to generate a four digital comparing signal DC4. Finally, a signal generator 66 will operate an adding/subtracting combination on the four digital comparing signals (in this embodiment, the adding/subtracting combination of the four digital comparing signals can be described as: DC2 + DC4 DC1 DC3) to generate the tracking error signal TE.

[0017] Although the above-mentioned prior art structures and methods for generating the tracking error signal TE are widely used, there is still room for improvement. First of all, in the embodiment shown in Fig.3, only the first digital detection signal D1 is delayed by the first digitizer 50, and the delayed first digital detection signal D1 is used as

a comparing criterion for the first digital detection signal D1 and the second digital detection signal D2. That is, the above-mentioned prior art neglects to put the second digital detection signal D2 into consideration when operating related delaying and comparing operations. Therefore, in some specific circumstances, the above-mentioned neglect will lead to an imbalance effect between signals. The imbalance effect will be aggravated in the embodiment shown in Fig.5.

[0018] In addition, when the optical drive changes its rotational speed, the frequency of an RF signal reproduced by the optical sensor 30 shown in Fig.2 (the RF signal can be treated as a sum of the four output signals a, b, c, d shown in Fig.2) will be correspondently changed, and the delay time of the first digitizer (50, 70) should be correspondently adjusted. Therefore, both the first digitizer 46 shown in Fig.3 and the first digitizer 64 shown in Fig.5 should be externally or internally installed with a tuning circuit to adjust the delay time according to the frequency of the RF signal. The installation of the tuning circuit, which is difficult for digital circuitry and is likely to increase the area of the first digitizer, is a great burden for the tracking error signal generator and the whole optical

storage system.

SUMMARY OF INVENTION

[0019] It is therefore a primary objective of the claimed invention to provide a method and related apparatus for deriving a tracking error signal based on a first analog detection signal and a second analog detection signal and to solve the above-mentioned problems.

[0020] In the claimed invention, an analog delay device is used to achieve a signal delay operation. The analog delay device can be an equalizer electrically connected to a digitizer, a relay, or an equalizer electrically connected to relay. Therefore, there is no need for installation of a tuning circuit to adjust the delay time. Moreover, combined with a synthesizer of the present invention, the optical sensor can generate a plurality of corresponding analog detection signals according to different detecting sections, and all of the analog detection signals corresponding to different portions of a light beam will be transmitted to the analog delay device. Therefore, all of the analog detection signals are in consideration when operating related delaying and comparing operations to erase an imbalance effect and to reduce the sensitivity for the delay time in the structure of the present invention.

[0021] According to the claimed invention, a method for deriving a tracking error signal based on a first analog detection signal and a second analog detection signal includes summing the first analog detection signal and the second analog detection signal into an analog sum signal. An analog delay device is used to delay the analog sum signal into a delay signal. The delay signal is digitized into a digital delay signal. The first analog detection signal and the second analog detection signal are respectively transformed into a first digital detection signal and a second digital detect signal. The digital delay signal is then compared with the first digital detection signal and the digital delay signal is then compared with the second digital detection signal to generate the tracking error signal.

[0022] According to the claimed invention, a method for deriving a tracking error signal in an optical storage system includes receiving an optical beam reflected and refracted via a recording carrier, the optical beam propagating along a track direction on the recording carrier according to the tracking error signal. According to a plurality of received different portions of the optical beam in space, a first analog detection signal and a second analog detection signal are generated where there is a time difference

between the first analog detection signal and the second analog detection signal. The first analog detection signal and the second analog detection signal are respectively transformed into a first digital detection signal and a second digital detect signal. The first analog detection signal and the second analog detection signal are summed into an analog sum signal. A delay operation is applied to the analog sum signal to be a delay signal. The delay signal is then digitized into a digital delay signal and respectively compared with the first digital detection signal and compared with the second digital detection signal to generate the tracking error signal.

[0023] According to the claimed invention, a tracking error signal generator used in an optical storage system for generating a tracking error signal includes two signal processing ports for respectively providing a first analog detection signal and a second analog detection signal where there is a time difference between the first analog detection signal and the second analog detection signal. A synthesizer is electrically connected to the two signal processing ports for synthesizing the first analog detection signal and the second analog detection signal into an analog sum signal. An analog delay device is electrically connected to the

synthesizer for delaying and digitalizing the analog sum signal into a digital delay signal. Two digitizers are electrically connected to the two signal processing ports for respectively transforming the first analog detection signal and the second analog detection signal into a first digital detection signal and a second digital detect signal. A comparing module is electrically connected to the analog delay device and the two digitizers for respectively comparing the digital delay signal with the first digital detection signal and comparing the digital delay signal with the second digital detection signal to generate the tracking error signal.

[0024] According to the claimed invention, a tracking error signal generator includes four signal processing ports for respectively providing a first analog detection signal, a second analog detection signal, a third analog detection signal, and a fourth analog detection signal. A synthesizer is electrically connected to the four signal processing ports for synthesizing the first analog detection signal, the second analog detection signal, the third analog detection signal, and the fourth analog detection signal into an analog summing signal. An analog delay device is electrically connected to the synthesizer for delaying and digitalizing

the analog summing signal into a digital delay summing signal. Four digitizers are respectively electrically connected to the four signal processing ports for respectively transforming the first analog detection signal, the second analog detection signal, the third analog detection signal, and the fourth analog detection signal into a first digital detect signal, a second digital detect signal, a third digital detect signal, and a fourth digital detect signal. A comparing module is electrically connected to the analog delay device and the four digitizers for applying a comparing operation to the digital delay summing signal respectively with the first digital detect signal, the second digital detect signal, the third digital detect signal, and the fourth digital detection signal to generate the tracking error signal.

[0025] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the various figures and drawings.

Brief Description of Drawings

[0026] Fig.1 is a schematic diagram of a typical optical drive.

[0027] Fig.2 is a schematic diagram showing a spatial relationship between a data track on the optical disk shown in Fig.1 and an optical sensor of the pick-up head.

[0028] Fig.3 is a functional block diagram of a tracking error signal generator according to the prior art.

[0029] Fig.4 is a time sequence diagram showing variations of a plurality of signals generated by the device of Fig.3.

[0030] Fig.5 is another functional block diagram of a tracking error signal generator according to the prior art.

[0031] Fig.6 is a functional block diagram of an embodiment of a tracking error signal generator according to the present invention.

[0032] Fig.7 is a flow chart of a method embodiment according to the present invention.

[0033] Fig.8 is a time sequence diagram showing variations in time domain of a plurality of signals generated by the device shown in Fig.6.

[0034] Fig.9 is a functional block diagram showing a detailed embodiment of the tracking error signal generator shown in Fig.6.

[0035] Fig.10 is a functional block diagram showing another embodiment of a tracking error signal generator according to the present invention.

[0036] Fig.11 is a functional block diagram of a detailed embodiment of the embodiment shown in Fig.10.

[0037] Fig.12 is a functional block diagram showing another embodiment of the tracking error signal generator according to the present invention.

DETAILED DESCRIPTION

[0038] The method and structure of the present invention is based on the structure of the optical sensor 30 (for generating a tracking error signal TE) in the above-mentioned prior art embodiment shown in Fig.2.Please refer to Fig.6, which is a functional block diagram of an embodiment of a tracking error signal generator 80 according to the present invention. The tracking error signal generator 80 is used in an optical storage system for generating a tracking error signal TE. The tracking error signal generator 80 includes a first signal processing port 82, a second signal processing port 84, a synthesizer 85, an analog delay device 90, a first digitizer 86, a second digitizer 88, and a comparing module 93. The first and second signal processing ports 82, 84 are respectively used to provide a first analog detection signal A1 and a second analog detection signal A2. Regarding the output signals a, b, c, d shown in Fig.2, the first analog detection signal A1 is

equal to a sum of the output signals a and the output signals c (A1≡ a+c), and the second analog detection signal A2 is equal to a sum of the output signals b and the output signals d (A2≡ b+d).

[0039] When the optical sensor 30 shown in Fig.2 (in the pick-up head 12 shown in Fig.1) deviates from the data track, there is a time difference between the first analog detection signal A1 and the second analog detection signal A2. One characteristic of the tracking error signal generator 80 according to the present invention is a synthesizer 85electrically connected to the two signal processing ports 82, 84. The synthesizer 85 can be used to synthesize the first analog detection signal A1 and the second analog detection signal A2 into an analog sum signal MA.

[0040] In addition, another important characteristic of the present invention is the installation of an analog delay device 90. The analog delay device 90, which is electrically connected to the synthesizer 85, can be used to delay/ digitalize the analog sum signal MA into a digital delay signal DR. The first and second digitizers86, 88, which are respectively electrically connected to the two signal processing port 82, 84, can be used to respectively transform the first analog detection signal A1 and the second analog

detection signal A2 into a first digital detection signal D1 and a second digital detection signal D2. Afterwards, the digital delay signal DR and the first digital detection signal D1 will pass through the comparing module 93, and in the meantime, the digital delay signal DR and the second digital detection signal D2 will also pass through the comparing module 93 to a comparing operation to generate the tracking error signal TE.

[0041] Please notice that the major characteristic of the tracking error signal generator 80 of the above-mentioned embodiment is to extract the time difference between the two analog detection signals (the first analog detection signal A1 and the second analog detection signal A2) to generate the tracking error signal TE. Therefore, the first analog detection signal A1 and the second analog detection signal A2 can be generated by any combination of the output signals a, b, c, d. That is, the combination of the output signals a, b, c, d (for generating the first analog detection signal A1 and the second analog detection signal A2) is only required to truly represent the deviation between a central spot of the optical beam (emitted from the optical sensor 30) on the recording carrier and the track direction.

[0042] Similarly, the tracking error signal generator 80 of the present invention is also suitable for other the optical sensors, such as a six-dimensional sensor, in addition to the four-dimensional sensor. Moreover, the synthesizer 85 of the present embodiment can be an adder for summing the first analog detection signal A1 and the second analog detection signal A2 to put these two analog detection signals into consideration of the related analog delay operation executed by the analog delay device 90.

[0043] Please notice that, the analog delay device 90 of the present invention can be implemented by an equalizer electrically connected to a digitizer, a relay, or an equalizer electrically connected to the relay. When being practically implemented, the equalizer, which can improve signal quality, is an initial element in the optical storage system of the present invention. Utilizing the equalizer to achieve the analog delay device 90 of the present invention can be used to adjust the delay time according to the frequencies of signals and saves circuitry area of the analog delay device 90. Moreover, the relay can also be used to adjust the delay time according to a predetermined voltage potential.

[0044] Therefore, when the frequency of signals read from a

recording carrier (as the optical disk 20 as shown in Fig.1) is high (the corresponding period is short in time domain), the determined delay time is short. Similarly, when the frequency of signals read from the recording carrier is low (the corresponding period is long in time domain), the determined delay time will be long. Thus, the analog delay device 90 implemented by a relay can dynamically determine corresponding proper delay times according to the frequencies of signals even in the high frequency domain.

[0045] Compared to the prior art technique shown in Fig.3, the tracking error signal generator 80 of the present embodiment can be treated as a mixed mode tracking error signal generator 80, which is implemented in neither a totally digital way nor a totally analog way. In brief, the mixed mode tracking error signal generator 80 of the present invention utilizes analog delay operations to simplify the signal delay operations and applies a digital signal operation to raise the accuracy of the generated tracking error signal TE.

[0046] According to the tracking error signal generator 80 in the above-mentioned embodiment shown in Fig.6, the present invention utilizing the first analog detection signal A1 and the second analog detection signal A2 to generate

the tracking error signal TE can be implemented with the following steps. Please refer to Fig.7, which is a flow chart of a method embodiment according to the present invention.

[0047] Step100: Add the first analog detection signal A1 with the second analog detection signal A2 to generate an analog sum signal MA.

[0048] Step101: Utilize the analog delay device 90 to delay the analog sum signal MA into a delay signal AR.

[0049] Step102: Digitalize the delay signal AR into a digital delay signal DR.

[0050] Step103: Respectively transform the first analog detection signal A1 and the second analog detection signal A2 into the first digital detection signal D1 and the second digital detection signal D2.

[0051] Step104: Execute a comparing operation (in the comparing module 93) toward the digital delay signal DR and the first digital detection signal D1, and in the meantime, execute a comparing operation (in the comparing module 93) toward the digital delay signal DR and the second digital detection signal D2 to generate the tracking error signal TE.

[0052] Please refer to Fig.9, which is a functional block diagram

showing a detailed embodiment of the tracking error signal generator 80 shown in Fig.6 to get a clear and detailed view of the inner operations of the tracking error signal generator 80 of the present invention. The first signal processing port 82 is used to transmit the output signal (a + c)(generated from the optical sensor 30 shown in Fig.2) to a first high-pass filter 81 to filter out the low-frequency noise and to get the first analog detection signal A1. The formula corresponding to the above-mentioned operation is:

$$A1 = G_{hpf}(a + c)$$

, where

$$G_{hpf}$$

is the transformation function of the first high-pass filter 81. Similarly, the second signal processing port 84 can be used to transmit the output signal (b + d) (generated from the optical sensor 30 shown in Fig.2) to a second high-pass filter 83 to generate the second analog detection signal A2. The corresponding operation formula is:

$$A2 = G_{h_{02}}(b + a)$$

, where

$G_{h_{02}}$

is the transformation function of the second high-pass filter 83 (

$G_{h_{02}}$

can be the same as or different to

$G_{h_{01}}$

).

[0053] Please refer to Fig.8, which is a time sequence diagram showing variations in time domain of a plurality of signals generated by an embodiment of the present invention illustrated in Fig.9. The plurality of signals include the first analog detection signal A1, the second analog detection signal A2, the analog sum signal MA, the delay signal AR, the digital delay signal DR, the first digital detection signal

D1, the second digital detection signal D2, a first comparing signal DC1, a second comparing signal DC2, a time-difference signal DT, and the tracking error signal TE. The synthesizer 85 shown in Fig.6 is implemented by an adder 87 in Fig.9, and the analog sum signal MA generated by the sum of the first and the second analog detection signal A1, A2 in the adder 87 (a normalized operation is also executed) is also shown in Fig.8. The first and second digitizer 86, 88 can be used to respectively transform the first and the second analog detection signal A1, A2 into the first digital detection signal D1 and the second digital detection signal D2, and the corresponding operation formulas can be respectively described as follows:

$$D1 = \begin{cases} 1 & A1 \geq 0 \\ 0 & A1 < 0 \end{cases}$$

;

$$D2 = \begin{cases} 1 & A2 \geq 0 \\ 0 & A2 < 0 \end{cases}$$

The analog delay device 90 of the present embodiment includes the equalizer 89 and the relay 91, and the analog sum signal MA (MA=A1+A2) will be transformed into the delay signal AR after being operated on by the equalizer 89. The corresponding operation formula is:

$$AR = f(A1, A2, \Delta\tau) = G_{eq}(A1 + A2) = \left|G_{eq}\right| e^{j\omega\Delta\tau}(A1 + A2)$$

, where

G_{eq}

is the transformation function the equalizer 89, and

$\Delta\tau$

is the delay time of the equalizer 89). After being operated by the relay 91, the delay signal AR becomes the digital delay signal DR, and the corresponding operation formula is:

$$DR = \begin{cases} 1 & AR \geq a \\ 0 & AR < -a \end{cases}$$

, where

a

is a predetermined voltage potential. The delay signal AR and the digital delay signal DR are all shown in Fig.8. The comparing module 93 includes a first comparator 92, a second comparator 94, an operator 96, and a low-pass filtering device 98.

[0054] The first comparator 92 and the second comparator 94 are respectively XOR (Exclusive OR) logic gates used for respectively extracting front edges and rear edges of the two input signals (the digital delay signal DR and the first digital detection signal D1, the digital delay signal DR, and the second digital detection signal D2). The digital delay signal DR and the first digital detection signal D1 will pass the first comparator 92 to generate the first comparing signal DC1 (the corresponding operation formula is:

$$DC1 = D1 \text{ xor } DR$$

). The digital delay signal DR and the second digital detection signal D2 will pass the second comparator 94 to generate the second comparing signal DC2 (the corresponding operation formula is:

$$DC2 = D2 \text{ xor } DR$$

). The operator 96 can be used to subtract the first comparing signal DC1 from the second comparing signal DC2 to generate the time-difference signal DT. Afterwards, the time-difference signal DT will pass the low-pass filtering device 98 to generate the tracking error signal TE, and the corresponding operation formula is:

$$TE = G_{lpf}(DC1 - DC2)$$

, where

G_{lpf}

is the transformation function of the low-pass filtering device 98.

[0055] After clarifying the major characteristics of the present invention, some important embodiments of the present invention will be introduced as follows. Please refer to Fig.10, which is a functional block diagram showing another embodiment of a tracking error signal generator 100 according to the present invention. Different from the embodiment shown in Fig.6, the present embodiment includes four signal processing ports 102 for respectively directly receiving the output signals a, b, c, and d of the

optical sensor 30 shown in Fig.2 and for assigning the four output signals a, b, c, and d respectively as a first analog detection signal A1, a second analog detection signal A2, a third analog detection signal A3, and a fourth analog detection signal A4.

[0056] The tracking error signal generator 100 of the present embodiment further includes a synthesizer 105, an analog delay device 110, four digitizers 104, and a comparing module 113. The synthesizer 105 is electrically connected to the four signal processing ports 102 and used to synthesize the first analog detection signal A1, the second analog detection signal A2, the third analog detection signal A3, and the fourth analog detection signal A4 into an analog summing signal AS. The analog delay device 110 is electrically connected to the synthesizer 105 for digitalizing/delaying the analog summing signal AS into a digital delay summing signal DSR. In the meantime, the four digitizers 104, which are electrically connected to the four signal processing ports 102, can be used to respectively transform the first analog detection signal A1, the second analog detection signal A2, the third analog detection signal A3, and the fourth analog detection signal A4 into a first digital detection signal D1, a second digital detection

signal D2, a third digital detection signal D3, and a fourth digital detection signal D4. Finally, the comparing module 113 will perform a comparing operation respectively on the digital delay summing signal DSR and the first digital detection signal D1, the digital delay summing signal DSR and the second digital detection signal D2, the digital delay summing signal DSR and third digital detection signal D3, and the digital delay summing signal DSR and the fourth digital detection signal D4 to generate the tracking error signal TE.

[0057] In brief, the characteristics of the present embodiment are similar to those shown in Fig.6. Compared to the prior art shown in Fig.5, the present embodiment, which synthesizes/sums a plurality of analog detection signals generated from the corresponding different detecting sections of the optical sensor 30 shown in Fig.2 and then delays and compares all those analog detection signals, can significantly improve the imbalance effect present in the prior art technique. In addition, utilizing the equalizer or/and the relay to achieve the analog delay device 110 can reduce the sensitivity required for estimating the accurate delay times in the present invention. Moreover, the analog delay device 110 of the present invention occupies less

circuitry area than the tuning circuit (combined with the digitizer) of the prior art.

[0058] Please refer to Fig.11, which is a functional block diagram of a detailed embodiment of the embodiment shown in Fig.10. The four signal processing ports 102 can be used to respectively receive the output signals a, b, c, d from the optical sensor 30 shown in Fig.2 and to transmit the output signals a, b, c, d to the four high-pass filters 103 to filter out the low-frequency noise. The first analog detection signal A1, the second analog detection signal A2, the third analog detection signal A3, and the fourth analog detection signal A4 are thus generated. The corresponding operation formulas are respectively:

$$A1 = G_{kp}(a)$$

;

$$A2 = G_{kp}(b)$$

;

$$A3 = G_{kp}(c)$$

;

$$A4 = G_{hp}(d)$$

, where

G_{hp}

is the transformation function of the four high-pass filters 103. When being practically implemented, the transformation functions of the four high-pass filters 103 are not required to be the same. Afterwards, the adder 107 shown in Fig.11, namely the synthesizer 105 shown in Fig.10, can be used to sum the first analog detection signal A1, the second analog detection signal A2, the third analog detection signal A3, and the fourth analog detection signal A4 into an analog summing signal AS.

[0059] The analog delay device 110 of the present embodiment also includes an equalizer 109 and a relay 111. The equalizer 109 can be used to delay the analog summing signal AS into a delay summing signal ASR. The corresponding operation formula is:

$$ASR = f(A1, A2, A3, A4, \Delta\tau) = G_{eq}(A1 + A2 + A3 + A4) = \left|G_{eq}\right| e^{j\Delta\varphi}(A1 + A2 + A3 + A4)$$

, where

G_{eq}

is the transformation function of the equalizer 109 and

$\Delta\tau$

is the delay time of the equalizer 109. The delay summing signal ASR will then pass the relay 111 to generate the digital delay summing signal DSR. The corresponding operation formula is:

$$DSR = \begin{cases} 1 & ASR \geq a \\ 0 & ASR < -a \end{cases}$$

, where

a

is a predetermined voltage potential.

[0060] In the meantime, the four digitizers 104 respectively transform the first, second, third, and fourth analog detection signals A1~A4 into the first digital detection signal D1, the second digital detection signal D2, the third digital detection signal D3, and the fourth digital detection

signal D4. The corresponding operation formulas can be respectively described as follows:

$$D1 = \begin{cases} 1 & A1 \geq 0 \\ 0 & A1 < 0 \end{cases}$$

;

$$D2 = \begin{cases} 1 & A2 \geq 0 \\ 0 & A2 < 0 \end{cases}$$

;

$$D3 = \begin{cases} 1 & A3 \geq 0 \\ 0 & A3 < 0 \end{cases}$$

;

$$D4 = \begin{cases} 1 & A4 \geq 0 \\ 0 & A4 < 0 \end{cases}$$

[0061] The comparing module 113 includes four comparators 108, an operator 116, and a low-pass filtering device 118. The four comparators 108 can be XOR logic gates for respectively extracting front edges and rear edges of the two input signals. The digital delay summing signal DSR and the first digital detection signal D1 will be compared to generate a first compare summing signal DSC1. The corresponding operation formula is:

$$DSC1 = D1 \text{ xor } DSR$$

. The digital delay summing signal DSR and the second digital detection signal D2 will be compared to generate a second compare summing signal DSC2. The corresponding operation formula is:

$$DSC2 = D2 \text{ xor } DSR$$

. The digital delay summing signal DSR and the third digital detection signal D3 will be compared to generate a third compare summing signal DSC3. The corresponding operation formula is:

$$DSC3 = D3 \text{ xor } DSR$$

. The digital delay summing signal DSR and the fourth

digital detection signal D4 will be compared to generate a fourth compare summing signal DSC4. The corresponding operation formula is:

$$DSC4 = D4 \text{ xor } DSR$$

.

[0062] The operator 116 can be used to add the first compare summing signal DSC1 with the third compare summing signal DSC3, and to subtract from the second compare summing signal DSC2 and the fourth compare summing signal DSC4. Finally, the calculated result of the operator 116 will be transmitted to the low-pass filtering device 118 to generate the tracking error signal TE, and the corresponding operation formula is:

$$TE = G_{lpf}(DSC1 - DSC2 + DSC3 - DSC4)$$

, where

G_{lpf}

is the transformation function of the low-pass filtering device 118.

[0063] Please refer to Fig.12, which is a functional block diagram showing another embodiment of a tracking error signal

generator 120 according to the present invention. The present embodiment emphasizes implementing an analog delay device 130 with only a relay 131. The basic structure is similar to the prior art embodiment shown in Fig.5, while the present embodiment inherits the characteristics of the present invention. The present embodiment still utilizes a mixed mode for implementing delay/compare operations instead of a totally digital way or a totally analog way to improve the prior art technique.

[0064] Similar to the embodiment shown in Fig.11, four signal processing ports 122 respectively receive the output signals a, b, c, d generated from the optical sensor 30shown in Fig.2 and respectively pass the four output signals to four high-pass filters 123 to filter out the low-frequency noise to get the first analog detection signal A1, the second analog detection signal A2, the third analog detection signal A3, and the fourth analog detection signal A4. The corresponding operation formulas are respectively:

$$A1 = G_{kp}(a)$$

;

$$A2 = G_{hp}(b)$$

;

$$A3 = G_{hp}(c)$$

;

$$A4 = G_{hp}(d)$$

, where

$$G_{hp}$$

is the transformation function of the four high-pass filters 123. The tracking error signal generator 120 of the present embodiment includes four digitizers 124, which are respectively electrically connected to the four signal processing ports 122 for respectively transforming the first, the second, the third, and the fourth analog detection signals A1~A4 into the first digital detection signal D1, the second digital detection signal D2, the third digital detection signal D3, and the fourth digital detection signal D4. The corresponding operation formulas are re-

spectively described as follows:

$$D1 = \begin{cases} 1 & A1 \geq 0 \\ 0 & A1 < 0 \end{cases}$$

;

$$D2 = \begin{cases} 1 & A2 \geq 0 \\ 0 & A2 < 0 \end{cases}$$

;

$$D3 = \begin{cases} 1 & A3 \geq 0 \\ 0 & A3 < 0 \end{cases}$$

;

$$D4 = \begin{cases} 1 & A4 \geq 0 \\ 0 & A4 < 0 \end{cases}$$

.

[0065] The present embodiment includes two relays 131. The relays 131 can be used to simply and dynamically determine proper delay times for different frequencies of signals and to digitalize the related delayed analog signals. Thus the two relays 131 can be used to respectively delay the first analog detection signal A1 and the third analog detection signal A3 into a first delay detection signal AR1 and a third delay detection signal AR3. The two relays 131 then respectively digitalize the first delay detection signal AR1 and third delay detection signal AR3 into a first digital delay detection signal DR1 and a third digital delay detection signal DR3.The corresponding operation formulas are

$$DR1 = \begin{cases} 1 & A1 \geq a \\ 0 & A1 < -a \end{cases}$$

and

$$DR3 = \begin{cases} 1 & A3 \geq a \\ 0 & A3 < -a \end{cases}$$

, where

is a predetermined voltage potential.

[0066] Afterwards, four comparators 128 (XOR logic gates) can be used as follows. The first digital delay detection signal DR1 is compared with the first digital detection signal D1 to generate a first digital comparing signal DC1(formula:

$$DC1 = D1 \text{ xor } DR1$$

). The first digital delay detection signal DR1 is compared with the second digital detection signal D2 to generate a second digital comparing signal DC2(formula:

$$DC2 = D2 \text{ xor } DR1$$

). The third digital delay detection signal DR3 is compared with the third digital detection signal D3 to generate a third digital comparing signal DC3(formula:

$$DC3 = D3 \text{ xor } DR3$$

). And, the third digital delay detection signal DR3 is compared with the fourth digital detection signal D4 to generate a fourth digital comparing signal DC4(the corresponding operation formula is:

$$DC4 = D4 \text{ xor } DR3$$

. An operator 136 will then operate a mathematical combination on the four digital comparing signals (DC1 + DC3 DC2 DC4), and finally a low-pass filtering device 138 can generate the tracking error signal TE. The corresponding operation formula is:

$$TE = G_{lpf}(DC1 - DC2 + DC3 - DC4)$$

, where

G_{lpf}

is the transformation function of the low-pass filtering device 138.

[0067] The time-difference extracting method and the tracking error signal generator of the present invention are suitable for various kinds of optical sensors, such as a multi-dimensional sensor, and various types of recording carriers, such as high-density or multi-layer optical disks. In contrast to the prior art techniques, first, the present invention sums all the analog detection signals generated by the optical sensor and puts all those analog detection

signals into the consideration when operating related delaying and comparing operations to erase an imbalance effect.

[0068] In addition, the present invention utilizes one or a plurality of analog delay devices to achieve analog signal delay operations. In the disclosed embodiments of the present invention, utilizing the initially installed equalizer (electrically connected to a digitizer), the relay, or the equalizer electrically connected to the relay to implement the analog delay device can simply and dynamically determine proper delay times for different frequencies of signals. Instead of the prior art technique of a totally digital approach by externally or internally installing a tuning circuit to adjust the delay time, the present invention applies the mixed (analog/digital) method to significantly save circuitry area used for executing related delay operations.

[0069] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.